REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update drawing to current requirements. Editorial changes throughout. gap	01-05-01	Raymond Monnin

REV																				
SHEET																				
REV	A	A	A	A	A	A	A	A	A	A										
SHEET	15	16	17	18	19	20	21	22	23	24										

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Tuan Nguyen

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Jeff Bowling

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
93-05-03

REVISION LEVEL
A

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 8K X 8 NON-VOLATILE STATIC RAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-93056**

SHEET 1 OF 24

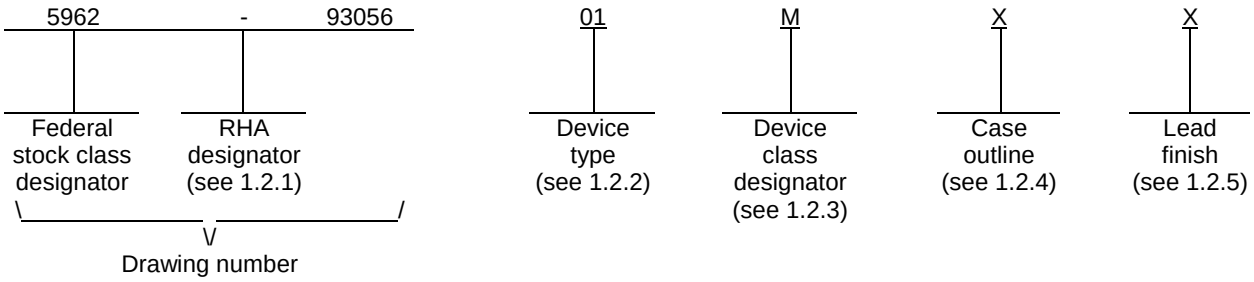
DSCC FORM 2233
APR 97

5962-E290-01

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access Time	Store Cycle	Recall Cycle	Endurance
01	10C68	8K X 8 NVSRAM	55 ns	12 ms	25 µs	10,000 cycles
02	10C68	8K X 8 NVSRAM	45 ns	12 ms	25 µs	10,000 cycles
03	10C68	8K X 8 NVSRAM	35 ns	12 ms	25 µs	10,000 cycles
04	10C68	8K X 8 NVSRAM	55 ns	12 ms	25 µs	100,000 cycles
05	10C68	8K X 8 NVSRAM	45 ns	12 ms	25 µs	100,000 cycles
06	10C68	8K X 8 NVSRAM	35 ns	12 ms	25 µs	100,000 cycles

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDIP3-T28 or GDIP4-T28	28	Dual-in-line
Y	CQCC3-N28	28	Rectangular leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/, 2/

Supply voltage range (V_{CC})	-0.6 V dc to 7.0 V dc
Voltage on DQ $_{(0-7)}$ with outputs in high Z state	-0.5 V to (V_{CC} + 0.5 V)
Input voltage operating range (V_{IH}, V_{IL})	-0.6 V dc to 7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Maximum output current	15 mA
Lead temperature (soldering)	300°C
Junction temperature (T_j) 3/	175°C
Thermal resistance, junction to case (θ_{jc}):	See MIL-STD-1835
Data retention	10 Years to nonvolatile array (minimum)
Endurance (as store cycles to non-volatile array)	Per 1.2.2

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Input voltage, low range (V_{IL})	V_{SS} -0.5 V dc to 0.8 V dc, all inputs
Input voltage, high range (V_{IH})	2.2 V dc to V_{CC} +0.5 V dc, all inputs

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may affect reliability. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied.
2/ All voltages are referenced to V_{SS} (ground).
3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DoDISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DoDISS are the issues of the documents cited in the solicitation.

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

JESD 78 - IC Latch-Up Test.

(Application for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

3.11 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase endurance cycles listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

3.12 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process changes which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ $V_{SS} = 0\ V$, $I_{OUT} = 0\ mA$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input leakage current (any input)	I_{IL}	$V_{CC} = 5.5\ V$ $V_{IN} = V_{SS}$ to V_{CC}	1, 2, 3	All		±1	µA
High impedance output leakage current	I_{OL}	$V_{CC} = 5.5\ V$ $V_{IN} = V_{SS}$ to V_{CC}	1, 2, 3	All		±5	µA
Input logic "1" voltage	V_{IH}	All Inputs	1, 2, 3	All	2.2	V_{CC} +.5	V
Input logic "0" voltage	V_{IL}	All Inputs	1, 2, 3	All	V_{SS} -.5	0.8	V
Output logic "1" voltage	V_{OH}	$I_{OH} = -4\ mA$	1, 2, 3	All	2.4		V
Output logic "0" voltage	V_{OL}	$I_{OL} = 8\ mA$	1, 2, 3	All		0.4	V
V_{CC} current 1/	I_{CC1}	Addresses cycling at t_{AVAV}	1, 2, 3	01, 04		70	mA
				02, 05		75	
				03, 06		80	
V_{CC} current 2/ during store cycle	I_{CC2}	$\overline{E} \ge (V_{CC} - 0.2V)$; all other inputs $V_{IN} \le 0.2\ V$ or $\ge (V_{CC} - 0.2\ V)$	1, 2, 3	All		50	mA
V_{CC} current (standby, cycling TTL input levels) 3/	I_{CC3}	$\overline{E} \ge V_{IH}$; all others cycling	1, 2, 3	01, 04		20	mA
				02, 05		23	
				03, 06		27	
V_{CC} DC current (standby, stable CMOS input levels) 2/	I_{CC4}	$\overline{E} \ge (V_{CC} - 0.2\ V)$; all others $V_{IN} \le 0.2\ V$ or $\ge (V_{CC} - 0.2V)$	1, 2, 3	All		2	mA
Input capacitance 4/	C_{IN}	$V_{IN} = 0\ V$ $T_A = 25°C$, f = 1.0 MHz See 4.4.1e	4	All		5	pF
Output capacitance 4/	C_{OUT}	$V_{OUT} = 0\ V$ $T_A = 25°C$, f = 1.0 MHz See 4.4.1e	4	All		7	pF
Functional test		See 4.4.1c	7, 8A, 8B	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ $V_{SS} = 0\ V$, $I_{OUT} = 0\ mA$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
READ CYCLES 1 & 2							
Chip enable access time	t_{ELQV}	See figures 3 and 4	9, 10, 11	01, 04		55	ns
				02, 05		45	
				03, 06		35	
Read cycle time 5/	t_{AVAV}		9, 10, 11	01, 04	55		ns
				02, 05	45		
				03, 06	35		
Address access time 6/	t_{AVQV}		9, 10, 11	01, 04		55	ns
				02, 05		45	
				03, 06		35	
Output enable to data valid	t_{GLQV}		9, 10, 11	01, 02		25	ns
				04, 05		25	
				03, 06		20	
Output hold after address change	t_{AXQX}		9, 10, 11	All	5		ns
Chip enable to output active	t_{ELQX}		9, 10, 11	All	5		ns
Chip disable to output inactive 7/	t_{EHQZ}		9, 10, 11	01, 02		25	ns
				04, 05		25	
				03, 06		20	
Output enable to output active	t_{GLQX}		9, 10, 11	All	0		ns
Output disable to output inactive 7/	t_{GHQZ}		9, 10, 11	01, 02		25	ns
				04, 05		25	
				03, 06		20	
Chip enable to power active 4/	t_{ELICCH}		9, 10, 11	All	0		ns
Chip disable to power standby 3/, 4/	t_{EHICCL}		9, 10, 11	All		25	ns
Write recovery time	t_{WHQV}		9, 10, 11	01, 04		65	ns
				02, 05		55	
				03, 06		45	
WRITE CYCLE 1							
Write cycle time	t_{AVAV}	See figures 3 and 4	9, 10, 11	01, 04	55		ns
				02, 03	45		
				05, 06	45		
Write pulse width	t_{WLWH}		9, 10, 11	01, 04	45		ns
				02, 03	35		
				05, 06	35		
Chip enable to end of write	t_{ELWH}		9, 10, 11	01, 04	45		ns
				02, 03	35		
				05, 06	35		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ $V_{SS} = 0\ V$, $I_{OUT} = 0\ mA$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data set-up to end of write	t_{DVWH}	See figures 3 and 4	9, 10, 11	All	30		ns
Data hold after end of write	t_{WHDX}		9, 10, 11	All	0		ns
Address set-up to end of write	t_{AVWH}		9, 10, 11	01, 04	45		ns
				02, 03	35		
				05, 06	35		
Address set-up to start of write	t_{AVWL}		9, 10, 11	All	0		ns
Address hold after end of write	t_{WHAX}		9, 10, 11	All	0		ns
Write enable to output disable 7/, 8/	t_{WLQZ}		9, 10, 11	All		35	ns
Output active after end of write	t_{WHQX}		9, 10, 11	All	5		ns
WRITE CYCLE 2							
Write cycle time	t_{AVAV}	See figure 3 and 4	9, 10, 11	01, 04	55		ns
				02, 05	45		
				03, 06	45		
Write pulse width	t_{WLEH}		9, 10, 11	01, 04	45		ns
				02, 05	35		
				03, 06	35		
Chip enable to end of write	t_{ELEH}		9, 10, 11	01, 04	45		ns
				02, 05	35		
				03, 06	35		
Data set-up to end of write	t_{DVEH}		9, 10, 11	All	30		ns
Data hold after end of write	t_{EHDX}		9, 10, 11	All	0		ns
Address set-up to end of write	t_{AVEH}		9, 10, 11	01, 04	45		ns
				02, 05	35		
				03, 06	35		
Address set-up to start of write	t_{AVEL}		9, 10, 11	All	0		ns
Address hold after end of write	t_{EHAX}		9, 10, 11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ $V_{SS} = 0\ V$, $I_{OUT} = 0\ mA$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
STORE CYCLE 1							
Array store cycle time 9/	t_{WLQX}	See figure 3 and 4	9, 10, 11	All		12	ms
Store initiation cycle time 10/	t_{WLNH}		9, 10, 11	All	55		ns
Output disable set-up to nonvolatile enable fall	t_{GHNL}		9, 10, 11	All	0		ns
Nonvolatile enable set-up	t_{NLWL}		9, 10, 11	All	0		ns
Chip enable set-up	t_{ELWL}		9, 10, 11	All	0		ns
STORE CYCLE 2							
Array store cycle time	t_{ELQXS}	See figure 3 and 4	9, 10, 11	All		12	ms
Store initiation cycle time	t_{ELNHS}		9, 10, 11	All	55		ns
Output disable set-up to chip enable fall	t_{GHEL}		9, 10, 11	All	0		ns
Nonvolatile enable set-up	t_{NLEL}		9, 10, 11	All	0		ns
Write enable set-up	t_{WLEL}		9, 10, 11	All	0		ns
RECALL CYCLE 1							
Array recall cycle time 11/	t_{NLQX}	See figure 3 and 4	9, 10, 11	All		25	µs
Recall initiation cycle 12/ time	t_{NLNH}		9, 10, 11	All	35		ns
Output enable set-up	t_{GLNL}		9, 10, 11	All	0		ns
Write enable set-up	t_{WHNL}		9, 10, 11	All	0		ns
Chip enable set-up	t_{ELNL}		9, 10, 11	All	0		ns
Nonvolatile enable fall to outputs inactive	t_{NLQZ}		9, 10, 11	All		35	ns

See footnotes at end of Table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ $V_{SS} = 0\ V$, $I_{OUT} = 0\ mA$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
RECALL CYCLE 2							
Array recall cycle time	t_{ELQXR}	See figure 3 and 4	9, 10, 11	All		25	µs
Recall initiation cycle time	t_{ELNHR}		9, 10, 11	All	35		ns
Nonvolatile enable set-up	t_{NLEL}		9, 10, 11	All	0		ns
Output enable set-up	t_{GLEL}		9, 10, 11	All	0		ns
Write enable set-up	t_{WHEL}		9, 10, 11	All	0		ns
RECALL CYCLE 3							
Array recall cycle time	t_{GLQXR}	See figure 3 and 4	9, 10, 11	All		25	µs
Recall initiation cycle time	t_{GLNH}		9, 10, 11	All	35		ns
Nonvolatile enable set-up	t_{NLGL}		9, 10, 11	All	0		ns
Output enable set-up	t_{GLNL}		9, 10, 11	All	0		ns
Write enable set-up 13/	t_{WHNL}		9, 10, 11	All	0		ns
Chip enable set-up	t_{ELGL}		9, 10, 11	All	0		ns

1/ I_{CC1} is dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
2/ I_{CC2} is the DC current required for the duration of the store cycle (t_{STORE}) once a store has begun.
3/ Bringing chip enable > V_{IH} will not produce standby current levels until any nonvolatile cycle in progress has timed out. See Figure 3.
4/ These parameters are tested as part of initial device characterization, and after any design or process change that might affect that parameter. These parameters are not tested as part of lot by lot screening, but are guaranteed to the limits specified in Table I.
5/ For read cycles 1 and 2, write enable is high for the entire cycle.
6/ The device is continuously selected with chip enable low and output enable low.
7/ Measured ±200 mV from steady state output voltage.
8/ If write enable is low when chip enable goes low, the outputs remain in the high impedance state.
9/ Measured with write enable and nonvolatile enable both returned high, and output enable returned low. Note that STORE cycles are inhibited/aborted by $V_{CC} < 3.8V$ (STORE Inhibit).
10/ Once t_{WC} has been satisfied by nonvolatile enable, output enable, write enable and chip enable, the STORE cycle is completed automatically. Any of nonvolatile enable, output enable, write enable or chip enable may be used to terminate the STORE initiation cycle.
11/ Measured with write enable and nonvolatile enable both high, and output enable and chip enable low.
12/ Once t_{NLNH} has been satisfied by nonvolatile enable, write enable, output enable and chip enable, the recall cycle is completed automatically. Any of nonvolatile enable, output enable or chip enable may be used to terminate the recall initiation cycle.
13/ For output enable controlled recall cycle 3, if write enable is low at any point in which both chip enable and nonvolatile enable are low and output enable is high, then a STORE cycle will be initiated instead of a RECALL.

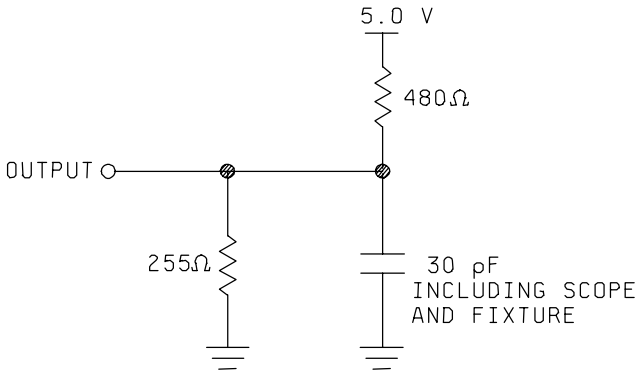
Device types	All
Case outlines	X, Y
Terminal number	Terminal symbol
1	$\overline{NE}$
2	A_{12}
3	A_7
4	A_6
5	A_5
6	A_4
7	A_3
8	A_2
9	A_1
10	A_0
11	DQ_0
12	DQ_1
13	DQ_2
14	V_{SS}
15	DQ_3
16	DQ_4
17	DQ_5
18	DQ_6
19	DQ_7
20	$\overline{E}$
21	A_{10}
22	$\overline{G}$
23	A_{11}
24	A_9
25	A_8
26	NC
27	$\overline{W}$
28	V_{CC}

FIGURE 1. Terminal connections.

$\overline{E}$	$\overline{W}$	$\overline{G}$	$\overline{NE}$	MODE	POWER
H	X	X	X	Not Selected	Standby
L	H	L	H	Read RAM	Active
L	L	X	H	Write RAM	Active
L	H	L	L	Nonvolatile Recall 1/	Active
L	L	H	L	Nonvolatile Store	I_{CC2}
L L	L H	L H	L X	No Operation	Active

FIGURE 2. Truth Table (Mode Selection, nonvolatile memory operation).

1/ An automatic RECALL also takes place at power up, starting when V_{CC} exceeds 3.8V, and taking t_{RECALL} from the time at which V_{CC} exceeds 4.5V. V_{CC} must not drop below 3.8V once it has exceeded it for the RECALL to function properly.



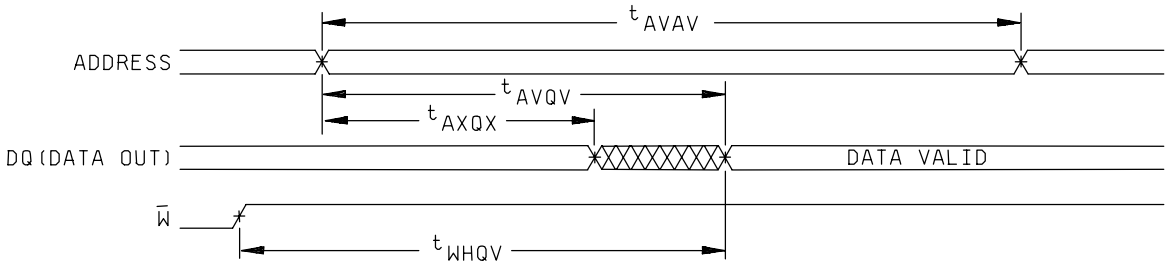
AC TEST CONDITIONS 1/

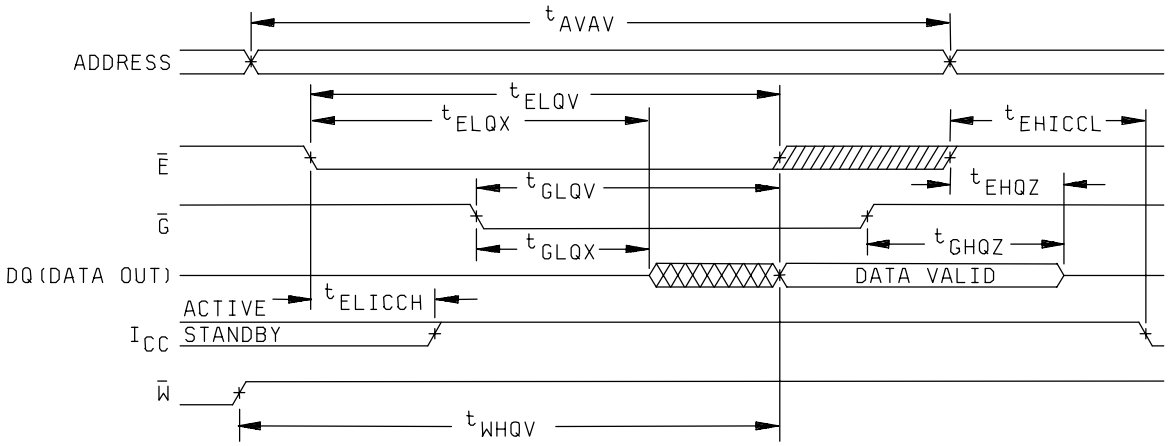
TEST CONDITION	VALUES
Input pulse levels	GND to 3V
Input rise & fall time	≤ 5 ns
Input timing reference levels	1.5V dc
Output reference levels	1.5V dc

1/ All voltages are referenced to V_{SS} (ground).

FIGURE 3. Output load circuits.

Read cycle 1 (see notes 1, 2, and 3)





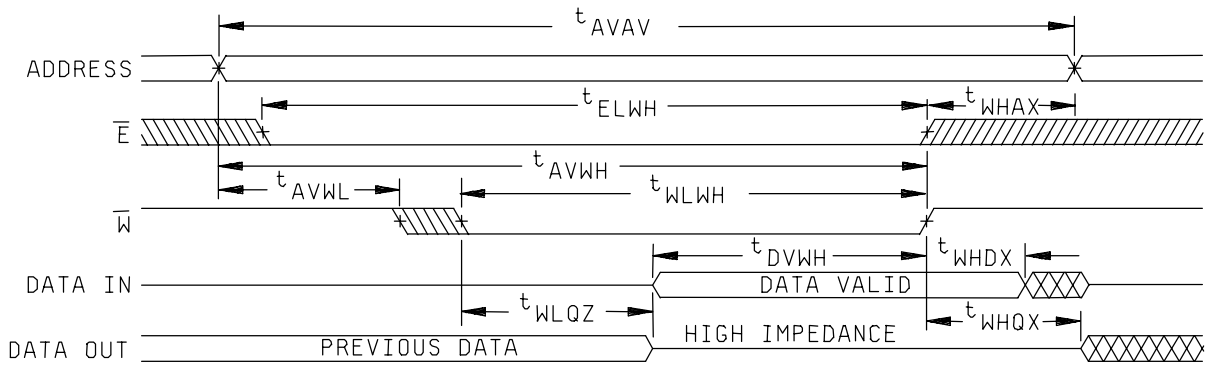
Read cycle 2 (see notes 1, 2, and 3)

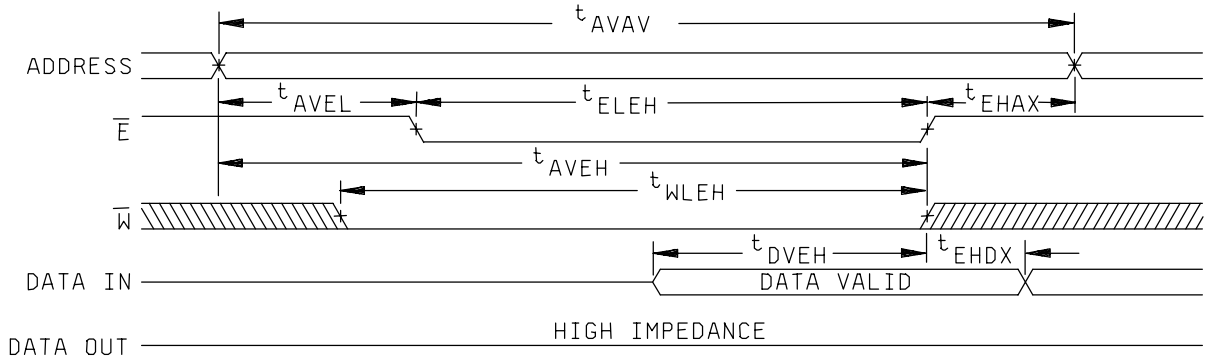
Notes:

1. The device is continuously selected with $\overline{E}$ low and $\overline{G}$ low.
2. For READ CYCLE #1 and #2, $\overline{W}$ and $\overline{NE}$ must be high for entire cycle.
3. Nonvolatile enable must be > V_{IH} during entire cycle.

Figure 4. Timing waveforms:

Write cycle 1: $\overline{W}$ controlled (see notes 1 and 2)



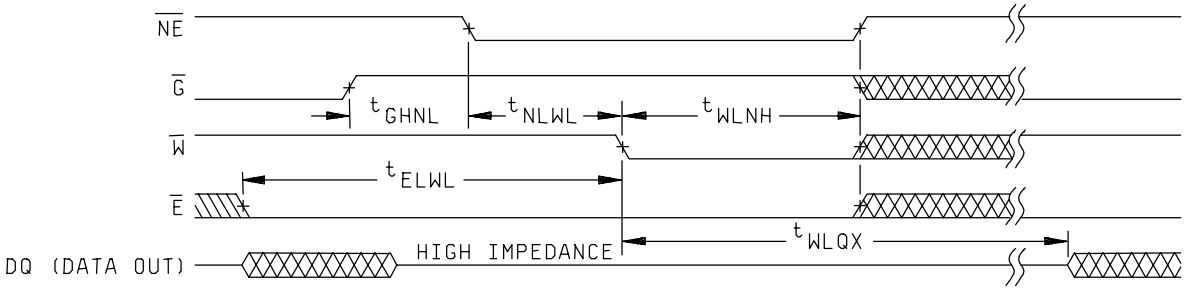


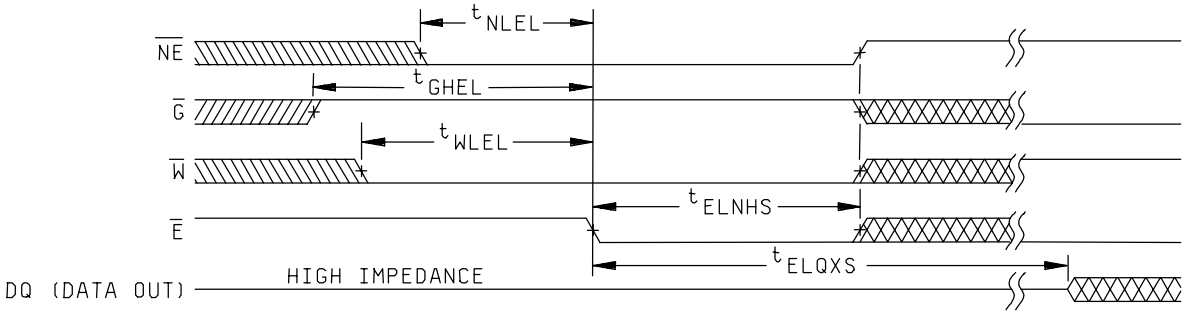
Write cycle 2: $\overline{E}$ controlled (see notes 1 and 2)

Notes:
1. $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
2. $\overline{NE}$ must be ≥ V_{IH} during entire cycle.

Figure 4. Timing waveforms - continued.

Store cycle 1: $\overline{WE}$ controlled (see note)





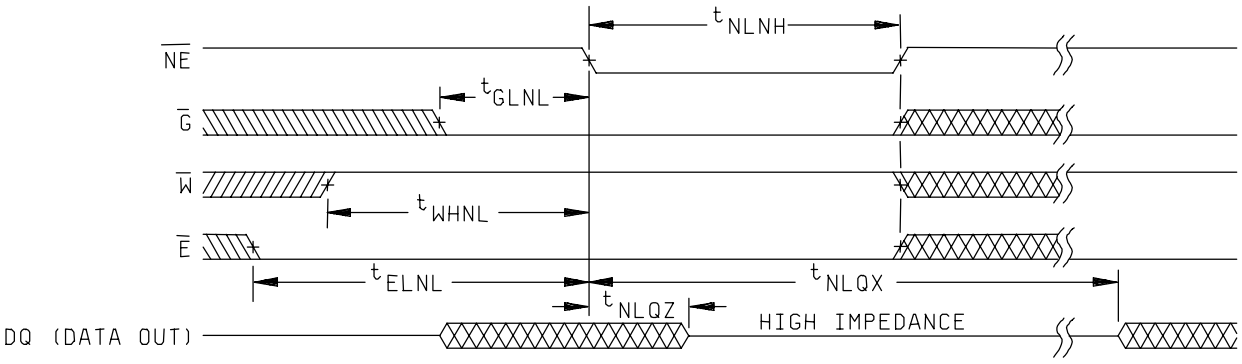
Store cycle 2: $\overline{CE}$ controlled (see note)

Note:

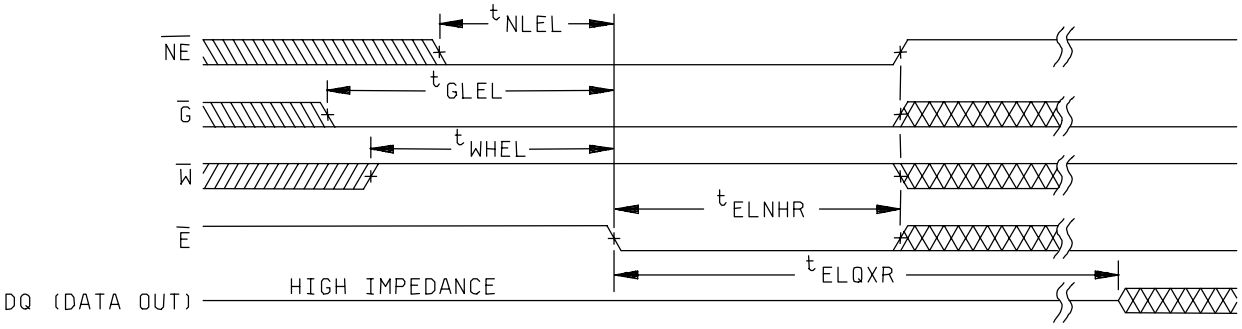
1. If $\overline{CE}$ is low for any period of time in which $\overline{WE}$ is high and $\overline{OE}$ and $\overline{NE}$ are low, then a recall cycle may be initiated.

Figure 4. Timing waveforms - continued.

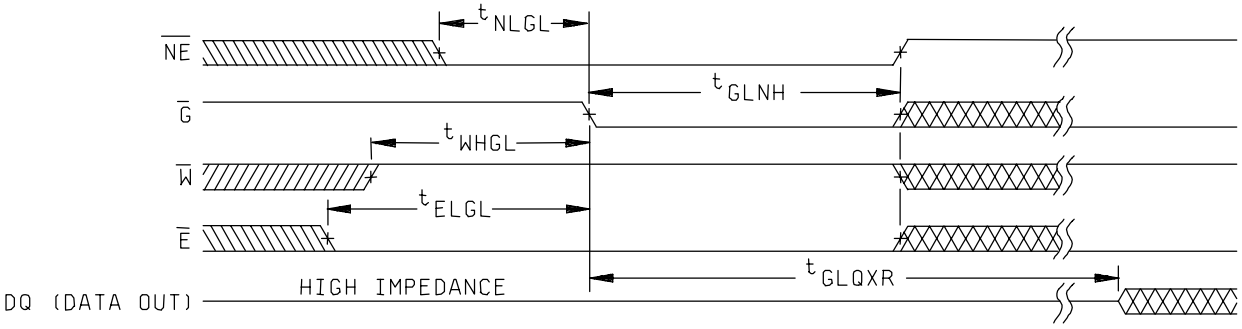
Recall cycle 1: $\overline{NE}$ controlled (see notes 1)



Recall cycle 2: $\overline{NE}$ controlled (see notes 1)



Recall cycle 3: $\overline{OE}$ controlled (see notes 1 and 2)



Notes:

1. If $\overline{E}$ is low for any period of time in which $\overline{W}$ is high and $\overline{G}$ and $\overline{NE}$ are low, then a recall cycle may be initiated.
2. For $\overline{G}$ controlled recall cycle #3, if $\overline{W}$ is low at any point in which both $\overline{E}$ and $\overline{NE}$ are low and $\overline{G}$ is high, then a store cycle will be initiated instead of a recall.

Figure 4. Timing waveforms - continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

TABLE IIA. Electrical test requirements.

	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1, 7, 9	1, 7, 9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point Electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B Δ	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types All
I_{CC4} standby	±10% value in table I
I_{IL}, I_{OL}	±10% value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device classes Q and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

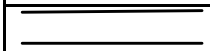
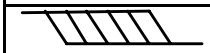
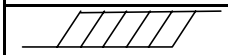
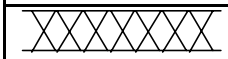
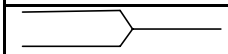
6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331 and as follows:

C_{IN}	.....	Input terminal capacitance.
C_{OUT}	.....	Output terminal capacitance.
GND	.....	Ground zero voltage potential.
I_{CC}	.....	Supply current.
I_{IH}	.....	Input high current.
I_{IL}	.....	Input low current.
T_C	.....	Case temperature.
T_A	.....	Ambient temperature
V_{CC}	.....	Ground zero voltage potential.
O/V	.....	Latch-up over-voltage
NE	.....	Nonvolatile enable

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).

30.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

30.2 Algorithm B (pattern 2).

30.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

30.3 Algorithm C (pattern 3).

30.3.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.

30.3.1 XY March - Continued.

Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

30.4 Algorithm D (pattern 4).

30.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-05-01

Approved sources of supply for SMD 5962-93056 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9305601MXA	3/	STK10C68-C55M
5962-9305601MYA	3/	STK10C68-L55M
5962-9305602MXA	3/	STK10C68-C45M
5962-9305602MYA	3/	STK10C68-L45M
5962-9305603MXA	3/	STK10C68-C35M
5962-9305603MYA	3/	STK10C68-L35M
5962-9305604MXA	0HMW2	STK10C68-5C55M
5962-9305604MXC	0HMW2	STK10C68-5C55M
5962-9305604MYA	0HMW2	STK10C68-5L55M
5962-9305605MXA	0HMW2	STK10C68-5C45M
5962-9305605MXC	0HMW2	STK10C68-5C45M
5962-9305605MYA	0HMW2	STK10C68-5L45M
5962-9305606MXA	0HMW2	STK10C68-5C35M
5962-9305606MXC	0HMW2	STK10C68-5C35M
5962-9305606MYA	0HMW2	STK10C68-5L35M

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0HMW2	Simtek Corporation 1465 Kelly Johnson Blvd Colorado Springs CO 80920